FIG. **14**A, if a high energy implant step, as described in application Ser. Nos. 07/855,373 and 07/854,162, is used to drive the dopant through the polysilicon gate. The sensitivity of the device characteristics to the level of epitaxial layer doping can be reduced by performing a second ion implantation (in addition to the counterdoping threshold voltage adjust) of the same conductivity type as the epitaxial layer itself. As shown in FIG. **14**G, a retrograde boron implant at a dosage in the range of 1×10^{12} to 5×10^{14} cm^{-2} is implanted at 200 kev or greater to a mean depth of 0.2 to 1.0 μm below the surface of the epitaxial layer, so that less surface counterdoping is needed. The unimplanted portion of the P-epitaxial layer may be thin or nonexistent (the retrograde layer can extend into the substrate. The advantages of using ion implantation to set the value of N_B and γ instead of using the epitaxial layer alone include improved dopant concentration control and the ability to select which MOSFETs in an IC are to be adjusted for pseudo-Schottky enhancement.

FIGS. **15**A–**15**C show a sequence of manufacturing steps that can be used to obtain a pseudo-Schottky synchronous rectifier based on a vertical DMOSFET. As shown in FIG. **15**A, an N-epitaxial layer **1512**, is grown on an N+ substrate **1510** which will be the cathode of the device. The doping level of the epitaxial layer is determined by the desired breakdown voltage of the device. For high voltage devices, concentrations of 1×10^{14} to 1×10^{15} cm^{-3} may be used while for lower voltages concentrations 1×10^{15} to 1633 10^{16} cm^{-3} may be employed. P-body regions **1514** are formed in N-epitaxial layer **1512** using conventional techniques. A gate oxide layer **1516** and a polysilicon gate **1518** are also formed using conventional techniques of implantation and drive-in.

FIG. **15**B shows the addition of N+ source regions **1522** and P+ body contact regions **1524**, also formed with conventional techniques. An N-type dopant **1520** (phosphorus) is then implanted at a dosage of 1×10^{11} to 1×10^{12} cm^{-2} and an energy of 300 keV to 2 MeV through gate **1518**. Dopant **1520** forms counter-doped threshold adjust regions **1528** (FIG. **15**C) at the surface of P-body regions **1514** in order to adjust the threshold voltage of the device. The phosphorous dopant will have little effect on the N-epitaxial layer **1512**, since it should be located near the surface. In FIG. **15**C the pseudo-Schottky synchronous rectifier **1590** is substantially completed by adding a metal source/body contact layer **1526**. Gate **1518** is electrically connected by a switch **1527** either to the source/body contact layer **1526** (when the device is in its pseudo-Schottky state) or to a source of gate drive voltage (when the device is in its MOSFET state).

FIG. **15**D shows the dopant concentration N_B of the device at a section taken along the dashed line in FIG. **15**C. In region A represents the N+ source region **1522**. Region B represents P-body region **1514**. The concentration near the surface of the body region, shown as a dashed line in FIG. **15**D, has been lowered due to the high energy counterdoping to adjust the threshold voltage V_t. Region C represents N-epitaxial layer **1512**, and Region D represents N+ substrate **1510**.

While specific embodiments in accordance with this invention have been described, these embodiments are to be considered as illustrative and not limiting. Numerous alternative embodiments will be apparent to those skilled in the art, all of which are within the broad scope of this invention. For example, the principles of this invention are equally applicable to other MOSFET structures such as lateral DMOS and cellular MOS structures, which have cells in square, hexagonal or other shaped cells, and for either N-channel or P-channel devices.

I claim:

1. A MOSFET comprising:

a first region of a first conductivity type;

a second region of a second conductivity type opposite to said first conductivity type adjacent said first region;

a third region of said first conductivity type adjacent said second region, wherein said first region and said second region are connected together and biased at a first voltage and said third region is biased at a second voltage, said first and second voltages being established such that a PN junction between said second region and said third region is forward-biased;

a gate separated by an insulating layer from a channel portion of said second region; and

a first switch for alternately connecting said gate to said first region or to a third voltage, said third voltage being sufficient to turn said MOSFET fully on.

2. The semiconductor device of claim **1** wherein an absolute value of said third voltage is greater than an absolute value of said first voltage.

3. A power converter comprising:

a MOSFET comprising:

a first region of a first conductivity type;

a second region of a second conductivity type opposite to said first conductivity type adjacent said first region;

a third region of said first conductivity type adjacent said second region, wherein said first region and said second region are connected together and biased at a first voltage and said third region is biased at a second voltage, said first and second voltages being established such that a PN junction between said second region and said third region is forward-biased;

a gate separated by an insulating layer from a channel portion of said second region; and

a first switch for alternately connecting said gate to said first region or to a third voltage, said third voltage being sufficient to turn said MOSFET fully on;

said power converter further comprising:

an inductor; and

a second switch connected in series with said inductor;

wherein said semiconductor device is connected to a common node between said inductor and said second switch.

4. The power converter of claim **3** further comprising a charge pump for supplying said third voltage.

5. The power converter of claim **3** wherein said first switch connects said gate to said first region during a break-before-make interval immediately after an opening of said second switch.

6. The power converter of claim **5** wherein said first switch connects said gate to said third voltage at a termination of said break-before-make interval.

7. A method of operating the power converter of claim **3** comprising the following sequence of steps:

maintaining said second switch in a closed condition while maintaining said first switch in a first position which connects said gate to said first region;

opening said second switch while maintaining said first switch in said first position; and

moving said first switch to a second position so as to connect said gate to said third voltage.

8. The method of claim **7** further comprising the step of using a charge pump to supply said third voltage.

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